# PAS2000

## TECHNICAL PRODUCT SPECIFICATION

## Van Ettinger Electronic Design

### REVISION HISTORY

| Date | Version | Author | Comments |
|---|---|---|---|
| 09-09-1999 | 0.1 | Norbert van Ettinger | Draft |
| 30-11-1999 | 0.2 | Norbert van Ettinger | Draft |
| 08-12-1999 | 0.3 | Norbert van Ettinger | Draft |
| 08-12-1999 | 0.4 | Norbert van Ettinger | Draft |
| 07-02-2000 | 0.5 | Norbert van Ettinger | Draft |
| 16-02-2000 | 0.6 | Norbert van Ettinger | Draft |
| 21-02-2000 | 0.7 | Norbert van Ettinger | Draft |
| 01-05-2000 | 0.8 | Norbert van Ettinger | Accepted |

## Table of Contents

# 1. INTRODUCTION

## 1.1 Purpose

This technical document describes the hardware of the PAS 2000 evolved from the Customer Requirement Specification ID: PAS2000_TD ( rev 0.03.000 dated 18-06-1999 ).

## 1.2 Scope

This document can be used as reference for development and product support.

## 1.3 Definitions, Acronyms and Abbreviations

| | |
|---|---|
| ADC | Analog Digital Converter |
| CTR | Current Transfer Ratio of opto coupler : Ic / If |
| DAC | Digital Analog Converter |
| dBm | 20 log ( Urms / 775 mV ) |
| PB | Play Back |
| REC | Recorder |
| VOX | Voice operated PTT switch |
| Vox spike immunity | Vox attack |
| µP | Micro processor / Micro controller |

## 1.4 References

| | | |
|---|---|---|
| P2000TPD.doc | This reference must be used for this document | |
| PAS 2000_TD | Concept technische beschrijving PAS 2000 | 0.003.000/18-06-99 |
| P2000HRS.doc | Hardware requirement specification | |
| P2mod30.doc | Modification document | |
| P2mthr30.uts | Mother board schematics (revision 3.0) | |
| P2ifan30.uts | Analog audio interface schematics (revision 3.0) | |
| P2telh30.uts | Telephone interface schematics (revision 3.0 ) | |

## 1.5 Summary

# 2. OVERALL BLOCK SCHEMATIC PAS2000

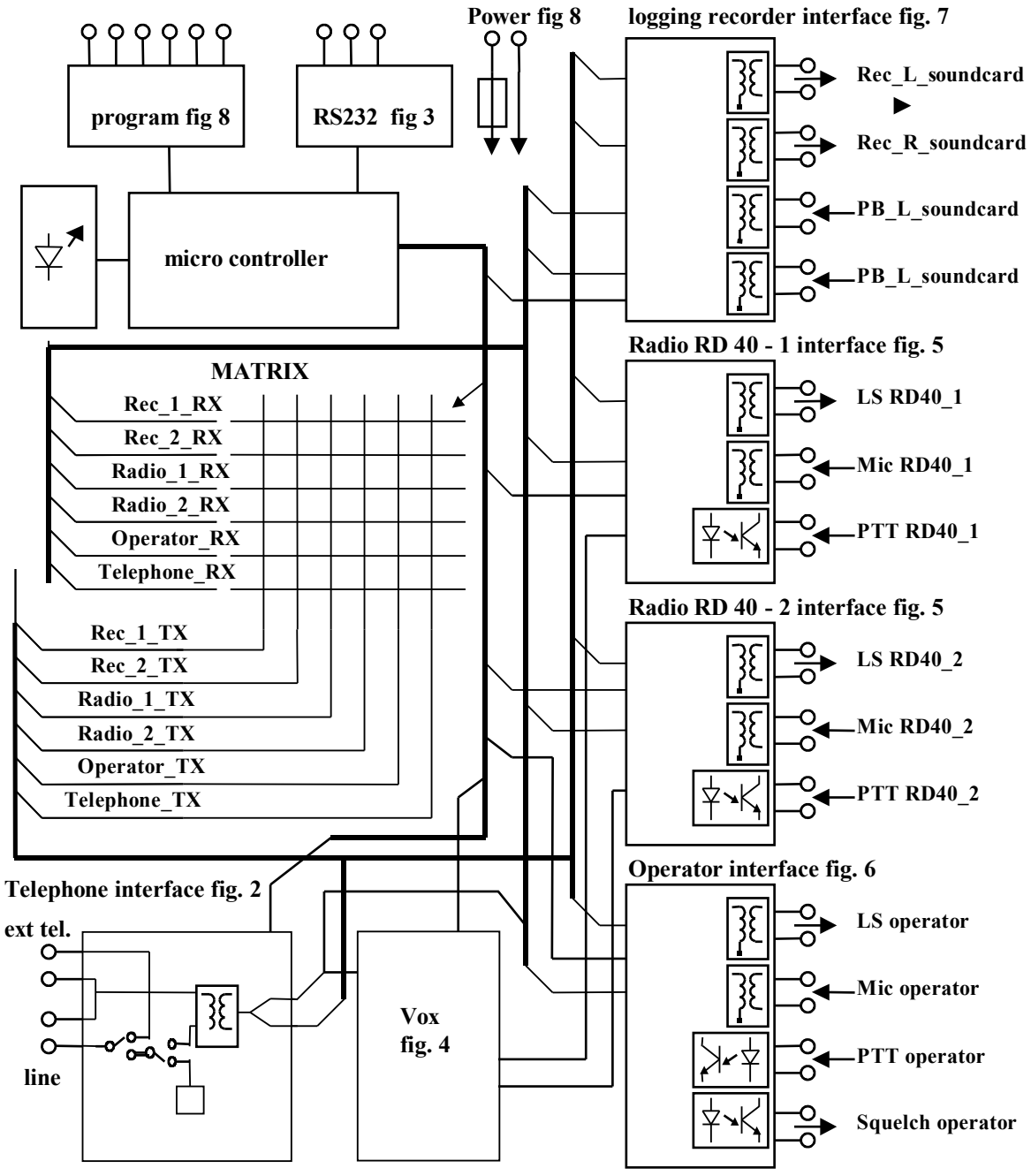



**Fig. 1) Overall Block schematic PAS 2000. Fig numbers referring t o P2000HRS.DOC**

# 3. INTERNAL CONTROL

## 3.1 Micro controller

| micro controller Atmel AT89S8252 ( 8051 derivate ) pin configuration | | | | | |
|---|---|---|---|---|---|
| µP pin | | Direction | configured | signal name | used for |
| Name | number | | as | acronyme | |
| P0.0 | 39 | Output | | STE_TX_DTMF | Sinlgle Tone enable DTMF |
| P0.1 | 38 | Output | | TGS_TX_DTMF | Tone Group Select DTMF |
| P0.2 | 37 | Output | | ETRE | External Telephone Relais |
| P0.3 | 36 | Output | | ELP (1) | serial Bus Enable latch potmeter |
| P0.4 | 35 | Output | | LEO# (1) | Output serial bus Latch enable 2 |
| P0.5 | 34 | Output | | LEI (1) | Input serial bus user input |
| P0.6 | 33 | Output | | RUN_LED | run led ( 0 => led on ) |
| P0.7 | 32 | Input | | PTT_OPRTR | Push To Talk OPerator |
| P1.0 | 1 | Input | | VTD | Vox Threshold Detect (1 => detect) |
| P1.1 | 2 | Output | | THRE | Telephone Hook ReLais |
| P1.2 | 3 | Input | | TRID | Telephone RIng detect |
| P1.3 | 4 | Output | | SQI | SQuelch Indication |
| P1.4 | 5 | Output | SS# | | |
| P1.5 | 6 | Output | mosi | SERDATO_SSB (2) | SERial DATa Output Serial Bus |
| P1.6 | 7 | Input | miso | SERDATI_SSB | SERial DATa Input Serial Bus |
| P1.7 | 8 | Output | sck | CLK_SSB (1,2) | CLocK Serial Bus |

1) These bus outputs are buffered with an hex schmitt trigger 74HC14. Therefore these signals are inverted available on the bus.

2) Bus signals buffered with two 74HC14 inverters in series. Therefore they are not inverted.

| micro controller Atmel AT89S8252 ( 8051 derivate ) pin configuration (continued) | | | | | |
|---|---|---|---|---|---|
| µP pin | | Direction | configured | signal name | used for |
| name | number | | as | acronyme | |
| P2.0 | 21 | Output | | CLR_CPD | CLeaR Call Progress Decoding |
| P2.1 | 22 | Output | | EN3ST_CPD | Enable 3 state Call Progress Dec |
| P2.2 | 23 | Output | | TE_TX_DTMF | Tone Enable TX-DTMF |
| P2.3 | 24 | Output | | TOE_RX_DTMF | Tone Output Enable RX DTMF |
| P2.4 | 25 | I/O | | TCTRL_DAT1 | Telephone Control |
| P2.5 | 26 | I/O | | TCTRL_DAT2 | Data bit 1 - 4 |
| P2.6 | 27 | I/O | | TCTRL_DAT3 | DTMF RX / TX and |
| P2.7 | 28 | I/O | | TCTRL_DAT4 | Call Progress |
| P3.0 | 10 | Input | RXD | RXD | RXD for RS232 |
| P3.1 | 11 | Output | TXD | TXD | TXD for RS232 |
| P3.2 | 12 | Input | interrupt 0 | VTR_DTMF | Valid tone received DTMF. |
| P3.3 | 13 | Input | interrupt 1 | VD_CPD | Valid data received Call Progress |
| P3.4 | 14 | Output | | ENVOX_RA1 | Vox Enable Radio 1 ( 1 => enabled ) |
| P3.5 | 15 | Output | | VDO_PTT_RA1 | Push To Talk radio 1 ( 1 => active ) |
| P3.6 | 16 | Output | | ENVOX_RA2 | Vox Enable Radio 2 ( 1 => enabled ) |
| P3.7 | 17 | Output | | VDO_PTT_RA2 | Push To Talk Radio 2 ( 1 => active) |

## 3.2 Serial synchronous peripheral addressing

### 3.2.1 Addressing the Matrix , the digital potmeters and the sensitivity of the input .

**General information** :
Used shift registers : 74HC4094. 8 stage (serial to parallel) shift - and - store bus register, having a storage latch associated with each stage for strobing data from the serial input D to the parallel buffered 3-state Outputs. The shift clock (pin 3) of these 74HC4094 shift registers is attached to the CLK_SSB# (idle is high) which is the buffered (by two inverters 74HC14 in cascade) serial bus line CLK_SSB = SPI_SCK pin P1_7 of micro controller AT89S8252 (idle is high => CPOL = 1 , CPHA = 1 ).
Shift register serial out-inputs are daisy chained. The serial input (pin 2 ) of an 74HC4094 is connected to the serial output (pin 10 ) of the previous one. The serial input pin of the first shiftregister is connected to the SPI_MOSI pin (SERDATO_SSB) of the microcontroller (AT89S8252). The output Latch enable input (pin 1) of each 74HC4094 is attached to a zero crossing circuit. This circuit produces a n high level (ZCLEn_SSB) when the audio input signal crosses zero level while the circuit is enabled by an active low ELP_SSB# line signal. ( ELP_SSB# , a line of the synchronous serial bus ,is the processor output pin 0.3 named ELP inverted and buffered by an 74HC14. Setting one of the controls (potmeter matrix or input sensitivity) can be done by modifying the right byte in the 24 byte train which has to be transmitted to the particular shift registers. When all the 24 bytes have been transmitted by the SPI interface, the ELP signal must be made High for the duration of 1/10 th of a second assuring the zero crossing circuit to give an latch enable high pulse (ZCLEn_SSB) to the shiftregister output latch at signal frequencies > 5 Hz at zero crossing. This Zero crossing circuit will anyhow produce an ZCLEn_SSB High puls when lifting the ELP_SSB# signal for the case in which the zero crossing did not occur within the 1/10th second time frame, therefore acting as safety net (safety strobe). for example at frequencies smaller than 5 Hz . There will be no sound click when the data already has been loaded, and only a small sound click for frequencies of < 5 Hz because the low part of the frequency band is subjected to cut off.

**SPI initialisation :**
Setting the SPI control register SPCR Address = 0xD5:

| SPI Control Register = SPCR | | | | |
|---|---|---|---|---|
| **Bitnumber** | **Accronyme** | **Description** | **Value** | |
| 7 msb | SPIE | SPI interrupt enable | 1 | interrupt enabled ! |
| 6 | SPE | SPI Enable | 1 | SPI enabled ! |
| 5 | DORD | Data Order | 0 | MSB first |
| 4 | MSTR | Master/slave select | 1 | Master |
| 3 | CPOL | Clock Polarity | 1 | SCK high when idle |
| 2 | CPHA | Clock Phase | 1 | |
| 1 | SPR0 | Clock rate | 0 | |
| 0 | SPR1 | Clock rate | 1 | |

## Transmission / activation controll

0) ELP = low (ELP_SSB# = High) , LEO# = High (LEO_SSB = Low)

1) write byte n ( start with byte 1 ) to SPDR *(SPI Data Register) (Place this command into an interrupt routine when the SPI interrupt is enabled)*
*The CPU starts the SPI clock generator and the data written shifts out of the CPU. After shifting one byte the SPI clock generator stops, setting the end of transmission flag (spif) . If both the SPI interrupt enable bit SPIE and the serial port interrupt are set an interrupt is requested . When the SPI interrupt is not used the SPIFbit in SPSR (SPI Status register) must be polled.*

2) When SPIF is set (or SPI interrupt 4 is requested) , write next byte to SPDR

3) Repeat steps 1 and 2 until all the 24 bytes have been written and transmission is completed (SPIE set).

4) Set ELP ( = resetting ELP_SSB#) for 100 milliseconds. ( ELP = 1 => 100 ms time elapse => ELP = 0 )
Below and in paragraph 12, the subsequent bytes and their controlling function is given . Byte number 1 is the first byte to send, byte number 24 the last one. The shift registers for controlling the matrix switches like the analog matrix switches are situated on the motherboard (mb). the shift registers for controlling the potentiometers and the analog matrix switches for adjusting the input sensitivity are situated on separate i / o audio interface pcb's (ai) (modules).

| **Byte 24 – 13 in first serial chain** | |
|---|---|
| **Byte number** | **control** |
| 24 | Matrix switches 1_1 – 1_6 |
| 23 | Matrix switches 1_2 – 6_2 |
| 22 | Matrix switches 1_3 – 6_3 |
| 21 | Matrix switches 1_4 – 6_4 |
| 20 | Matrix switches 1_5 – 6_5 |
| 19 | Matrix switches 1_6 – 6_6 |
| 18 | Play back attenuation control |
| 17 | Recorder 1 attenuation control |
| 16 | Recorder 2 attenuation control |
| 15 | Play back 2 gain control |
| 14 | Play back 1 gain control |
| 13 | Play back 2 attenuation control |

| **Byte 13 – 1 in first serial chain** | |
|---|---|
| **Byte number** | **Control** |
| 12 | RX radio 1 attenuation control |
| 11 | Tx radio1 attenuation control |
| 10 | Tx radio2 attenuation control |
| 9 | RX radio 2 gain control |
| 8 | RX radio 1 gain control |
| 7 | RX radio 2 attenuation control |
| 6 | Mic operator attenuation ctrl |
| 5 | LS operator attenuation ctrl |
| 4 | TX telephone attenuation ctrl |
| 3 | RX telephone attenuation ctrl |
| 2 | Mic operator gain control |
| 1 | RX telephone attenuation ctrl |

Data Shifting (transmission of bytes via the SPI bus) on the SSB is only allowed when **none** of the latch signals is active to avoid data being placed into the wrong shifregisters. ( ELP= active High, LEO# = active low, LEI = active high). Wait after an ELP reset strobe , minimal 5 * 100 K * 2.2 N = 1.1 milli seconds giving ZCLE_SSB_n this time to generate the safety strobe ,before transmitting the next byte train out of Mosi into the shift registers.

### 3.2.2 Addressing outputs in the second serial shift register chain

Latch signal LEO_SSB ,which is the inverted / buffered LEO# signal of processor output pin P0.4 , is addressing the output latches of the 74HC4094 shift registers from :

- the test hex displays
- the 8 * user outputs with opto couplers
- The Vox Threshold DAC
- The VOX spike immunity DAC ( = Vox Attack DAC)

The shift clock (pin 3) of these 74HC4094 shift registers is attached to the CLK_SSB# (idle is high) which is the buffered (by two inverters 74HC14 in cascade) serial bus line CLK_SSB = SPI_SCK pin P1_7 of micro controller AT89S8252 (CPOL=1,idle is high, CPHA = 1 ). Serial data of the first 74HC4094 (pin 2) is provided by the serial DATA bus line SERDATO_SSB = SPI_MOSI controller pin P1_5. The 4094 data output pin 10 is connected to the serial data input pin (2) of the subsequent shift register. (data line is daisy chained) . Writing the parallel outputs of the shift registers happens by first serial loading all the subsequent bytes into the flip flops of all the daisy chained shiftregister in the branch followed by an low pulse LEO# = High pulse LEO_SSB.

**SPI initialisation :**
Same as under 3.2.1 .

**Transmission / activation control**

0) LEO# = High (LEO_SSB = Low), ELP = low (ELP_SSB# = High)

1) write byte n ( start with byte 1 ) to SPDR (SPI Data Register) (Place this command into an interrupt routine when the SPI interrupt is enabled)
The CPU starts the SPI clock generator and the data written shifts out of the CPU. After shifting one byte the SPI clock generator stops, setting the end of transmission flag (spif) . If both the SPI interrupt enable bit SPIE and the serial port interrupt are set an interrupt is requested . When the SPI interrupt is not used the SPIFbit in SPSR (SPI Status register) must be polled.

2) When SPIF is set (or SPI interrupt 4 is requested) , write next byte to SPDR

3) Repeat steps 1 and 2 until all the 5 bytes have been written and transmission is completed (SPIE set).

4) Reset LEO# ( = setting LEO_SSB) for 10 milliseconds. ( LEO# = 0 => 10 ms time elapse => LEO# = 1 )

| Byte 5 – 1 in second serial chain | |
|---|---|
| **Byte number** | **Control** |
| 5 | Left Hex Display |
| 4 | Right Hex Display |
| 3 | Opto couplers for user outputs |
| 2 | Vox threshold DAC |
| 1 | Vox attack DAC |

### 3.2.3 Addressing the inputs in the third serial shift register chain

Latch signal LEI_SSB# ,which is the inverted and buffered LEI signal of processor output pin P0.5 , is addressing the input latches of the 74HC7597 (parallel to serial) shift registers from :

* the 8 bit user opto coupler input
* the 8 bit Test input ,with pull up resistors, connected to a dipswitch .
* the 8 bit Test input ,with pull up resistors, connected to for example a keyboard

The shift clock (pin 13) of the 74HC7597 shift registers is attached to the CLK_SSB (idle is low which is the inverted SPI_SCK pin P1_7 signal of micro controller AT89S8252 (CPOL=1, idle is high, CPHA = 1, ). The 74HC7597 parallel to serial shift registers are daisy chained meaning that the serial data output (pin 9 ) of the first shift register is connected (via an extra flip flop) to the micro controller pin 'miso' = SERDATI_SSB , the serial data output of the second shift register connected to the serial input (pin 14) of the first shift register , etc. Reading the inputs happens by first generating a High pulse on LEI ( = low pulse on LEI_SSB# ) followed by 3 times a dummy byte write or by writing the byte train to the potentiometer chain or to the other outputs. After the first (dummy) byte ,has been transmitted the first received input byte (Byte 1 ) can be taken from the serial data register. The same procedure must be followed for the second and third input byte .

**SPI initialisation :** Same as under 3.2.1 .

### Transmission / activation control

**0) Set LEI (= resetting LEI_SSB# ) for 10 milliseconds.** ( LEI = 1 => 10 ms time elapse => LEI = 0 )
**1) LEO# = High (LEO_SSB = Low), ELP = low (ELP_SSB# = High)**

**2) Write a (dummy) byte to SPDR (SPI Data Register)** *(Place this command into an interrupt routine when the SPI interrupt is enabled) . The CPU starts the SPI clock generator and the (dummy) byte written to the SPDR shifts out of the CPU. After shifting one byte the SPI clock generator stops, setting the end of transmission flag (spif) . If both the SPI interrupt enable bit SPIE and the serial port interrupt are set an interrupt is requested . When the SPI interrupt is not used the SPIFbit in SPSR (SPI Status register) must be polled.. When SPIF is set (or SPI interrupt 4 is requested) , the SPDR contains the input variable which was shifted in via miso while the (dummy) byte was shifted out through mosi .*

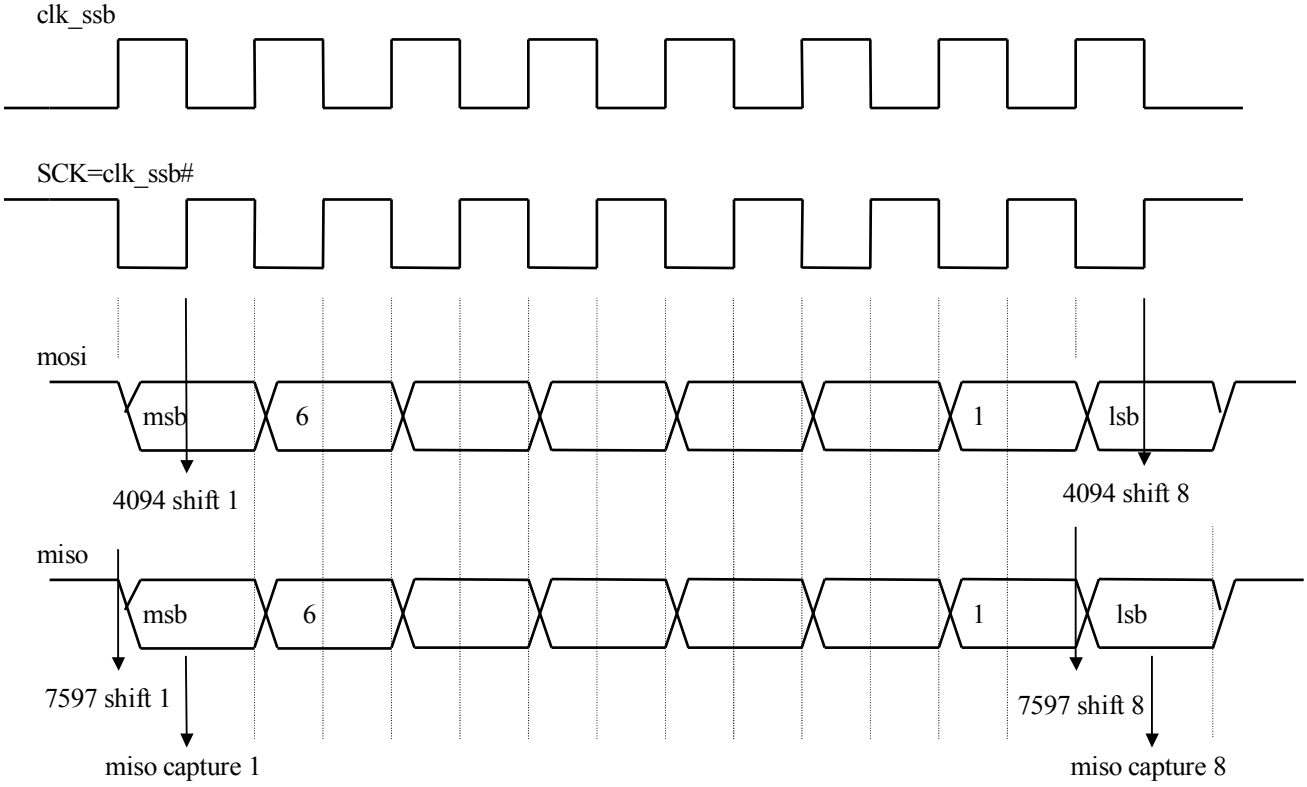
**3) Copy the SPDR contents into the proper variable.** *The sequence of entrance is : after the first (dummy) byte write the SPDR contains the USER input byte, after the second it contains the Dipswitch and after the third the test input byte.*

**4) Write the next byte to SPDR**

**5) Repeat steps 2 to 4 until all the input bytes have been received** and when combined with writing serial output shift register chain 1 or 2 until this transmission is completed .

| Byte 1 – 3 in third serial input chain | |
|---|---|
| **Byte number** | **Control** |
| 1 | User input opto couplers |
| 2 | Dipswitch |
| 3 | Test inputs |

### 3.2.4 SPI addressing




SPI addressing , CPOL = 1, CPHA = 1

## 3.3 Input sensitivity (gain) control

| INPUT SENSITIVITY ( INPUT GAIN ) | | | | | | | |
|---|---|---|---|---|---|---|---|
| INPUT GAIN CONTROL BITS = | | | | GAIN CTRL BYTE | | GAIN | |
| ISYn3 | ISYn2 | ISYn1 | ISYn0 | DEC. | HEX | Linear | dB |
| 1 | ( 0 ) | ( 0 ) | ( 0 ) | 8 | 0x08 | 82.0 | +38.3 |
| 0 | 1 | 1 | ( 0 ) | 6 | 0x06 | 29.1 | +29.3 |
| 0 | 1 | 0 | ( 0 ) | 4 | 0x04 | 10.3 | +20.3 |
| 0 | 0 | ( 0 ) | 1 | 1 | 0x01 | 3.7 | +11.3 |
| 0 | 0 | ( 0 ) | 1 | 0 | 0x00 | 1.3 | +2.3 |

( 0 ) means don't care !

| GAIN SETTING INPUT SENSITIVITY PAS 2000 | | | | | | |
|---|---|---|---|---|---|---|
| REQUIRED | | GAIN SETTINGS | | | | |
| Input description | expected nominal level | CTRL byte | Gain linear | Gain dB | input Impedance | Input Resistor analog i/o interface |
| logging PB | +4 dBu @600Ω | 0x00 | 1.3 | +2.3 | 600Ω | R117 = 680R R56 = 680R |
| RD40 LS | -13.7 dBu @600Ω | 0x04 | 10.3 | +20.3 | 600Ω | R117 = 680R R56 = 680R |
| Operator | +3 dBu @600Ω | 0x00 | 1.3 | +2.3 | 600Ω | R117 = 680R R56 = 680R |
| Telephone RX | | | | | | |

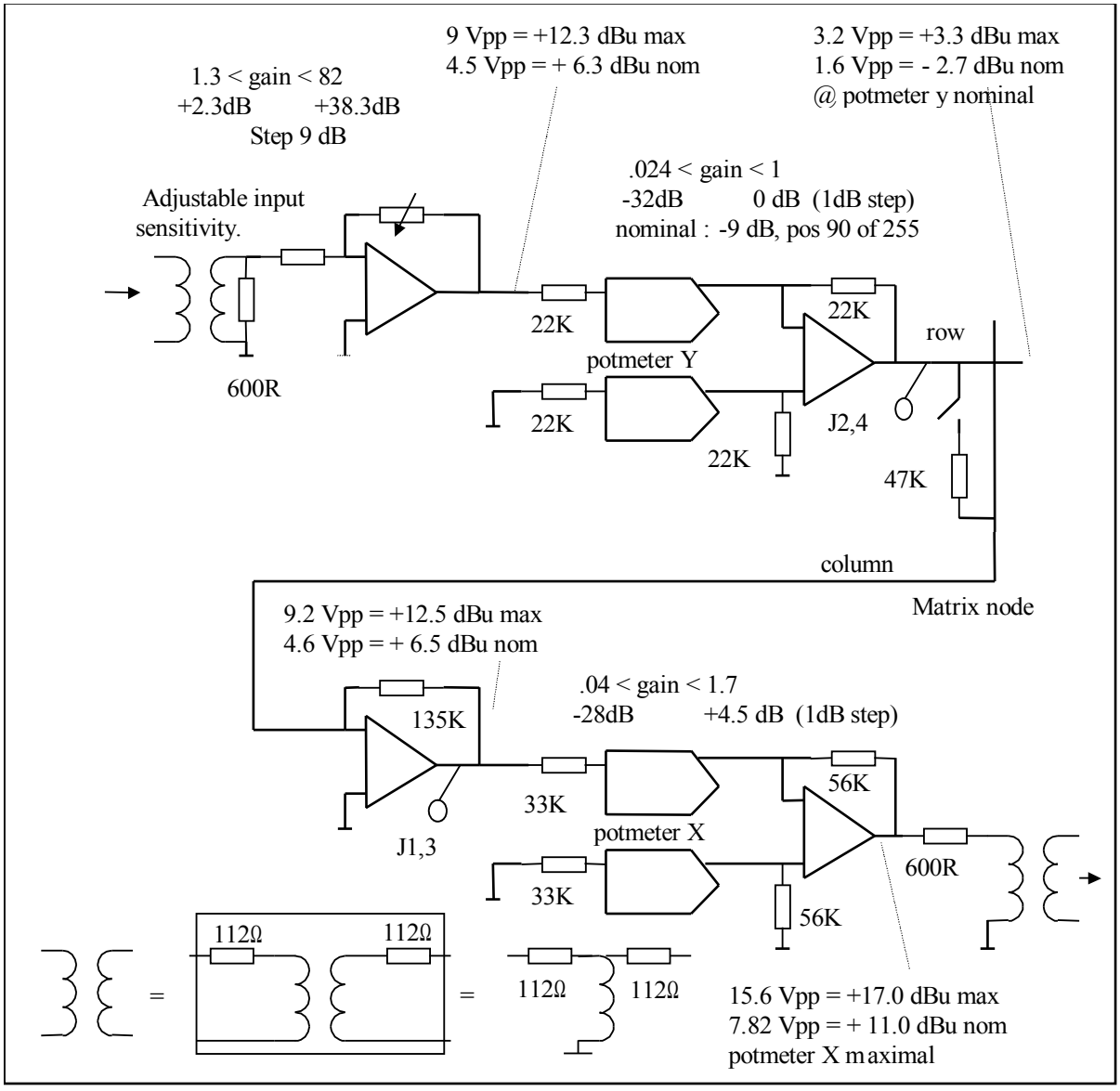
Maximum level 6 dB above nominal signal is just not clipping.

## 3.4 Attenuation Control

Concerning the digital control of the potentiometer (DAC08) .

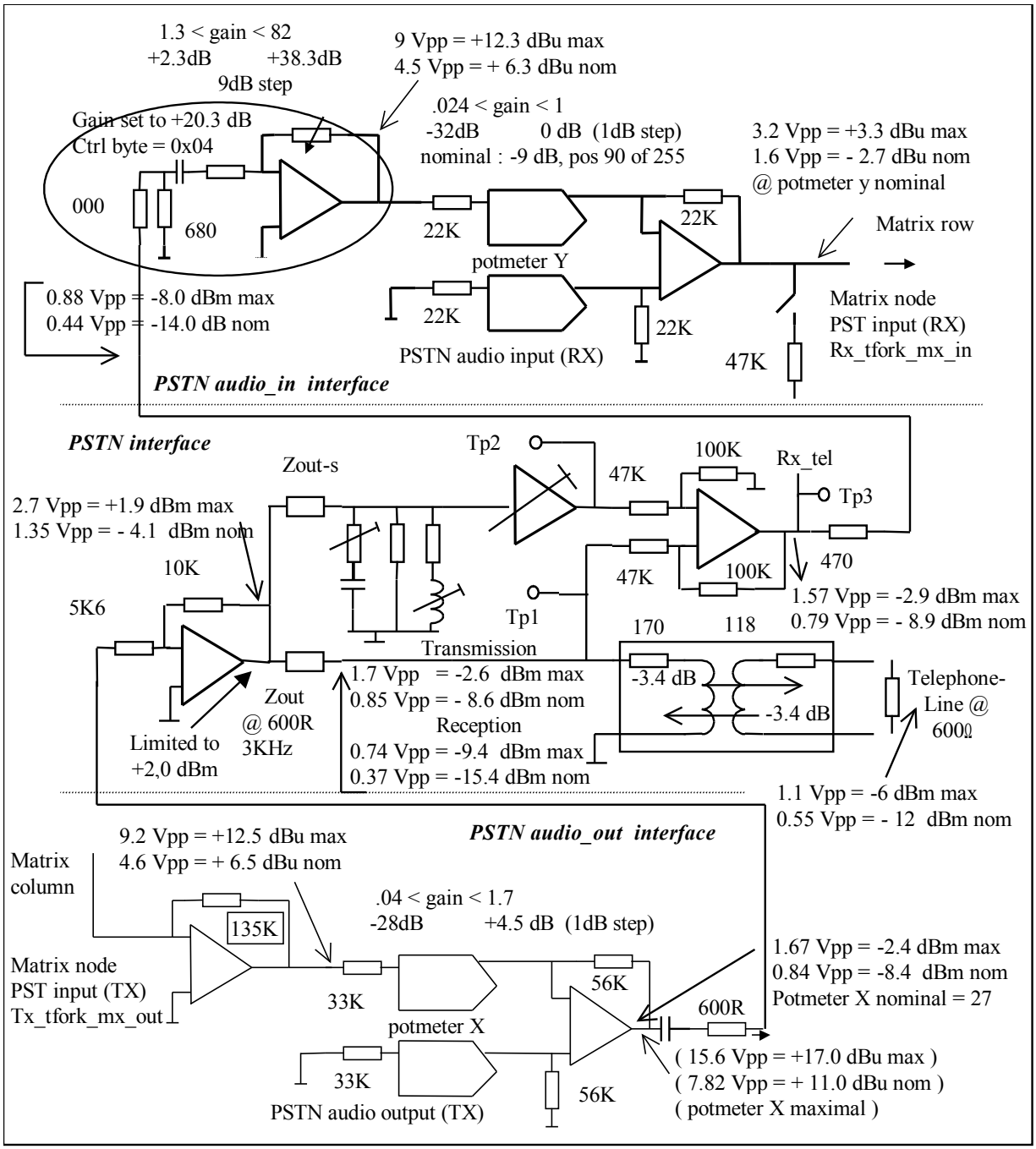
| Gain dB | Gain linear | linear position | ctrl byte hex | Gain dB | Gain linear | linear position | ctrl byte hex |
|---|---|---|---|---|---|---|---|
| 0 | 1.0 | 255 | 0xff | -21 | 0.090 | 23 | 0x17 |
| -1 | 0.89 | 226 | 0xe2 | -22 | 0.078 | 20 | 0x14 |
| -2 | 0.79 | 201 | 0xc9 | -23 | 0.071 | 18 | 0x12 |
| -3 | 0.71 | 180 | 0xb4 | -24 | 0.063 | 16 | 0x10 |
| -4 | 0.63 | 160 | 0xa0 | -25 | 0.055 | 14 | 0x0e |
| -5 | 0.56 | 143 | 0x8f | -26 | 0.051 | 13 | ox0d |
| -6 | 0.50 | 127 | 0x7f | -27 | 0.043 | 11 | 0x0b |
| -7 | 0.44 | 113 | 0x71 | -28 | 0.039 | 10 | 0x0a |
| -8 | 0.39 | 100 | 0x64 | -29 | 0.036 | 9 | 0x09 |
| -9 | 0.35 | 90 | 0x5a | -30 | 0.031 | 8 | 0x08 |
| -10 | 0.31 | 80 | 0x50 | -31 | 0.027 | 7 | 0x07 |
| -11 | 0.28 | 72 | 0x48 | -32 | 0.024 | 6 | 0x06 |
| -12 | 0.25 | 64 | 0x40 | *-34* | *0.020* | *5* | *0x05* |
| -13 | 0.22 | 57 | 0x39 | *-36* | *0.016* | *4* | *0x04* |
| -14 | 0.20 | 51 | 0x33 | *-39* | *0.012* | *3* | *0x03* |
| -15 | 0.18 | 45 | 0x2d | *-42* | *0.008* | *2* | *0x02* |
| -16 | 0.16 | 40 | 0x28 | *-48* | *0.004* | *1* | *0x01* |
| -17 | 0.14 | 36 | 0x24 | *-infinit* | *0* | *0* | *0x00* |
| -18 | 0.13 | 32 | 0x20 | | | | |
| -19 | 0.11 | 29 | 0x1D | | | | |
| -20 | 0.10 | 25 | 0x19 | | | | |

# 4. LEVEL DIAGRAM AUDIO INTERFACE

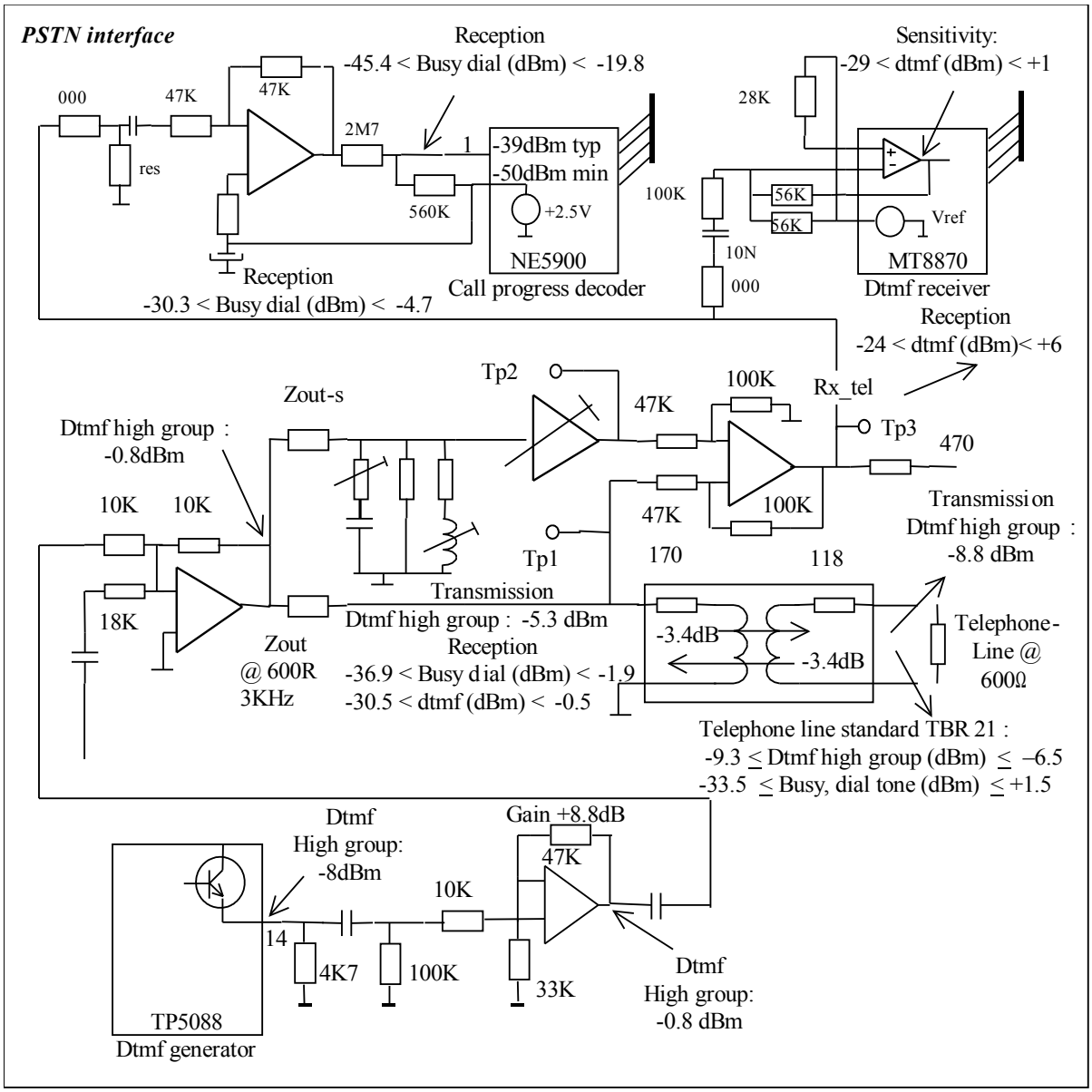



When n signals of n rows will be mixed together in the matrix , reduce the signal level on the row with 20log(√n) . This can be done by adapting the gain of the adjustable input and / or by adjusting the attenuation , both in the input chain.

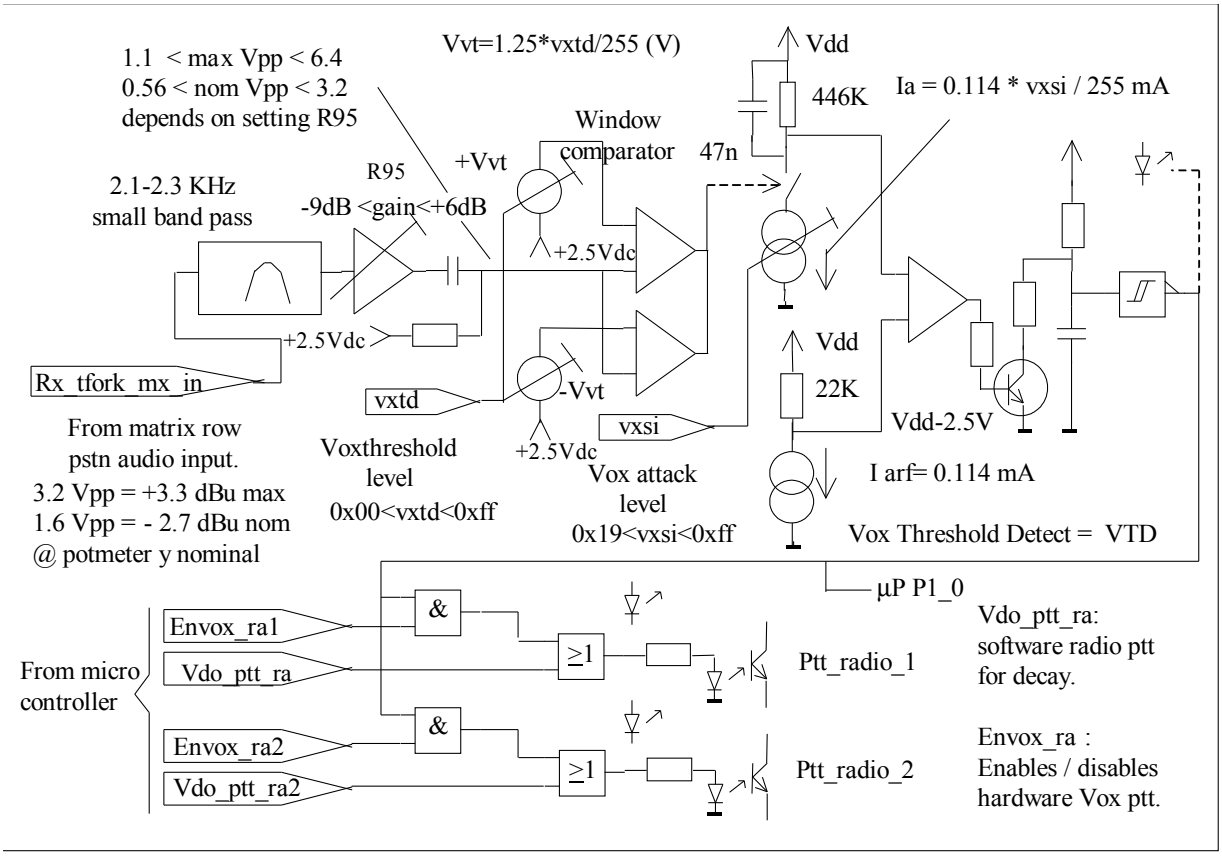
# 5. TELEPHONE INTERFACE AUDIO LEVEL DIAGRAM



# 6. TELEPHONE INTERFACE CONTROL LEVELS



# 7. VOICE OPERATED SWITCH LEVEL DIAGRAM.




**TECHNICAL SPECIFICATIONS :**

**Vox threshold** :

R95 adjusted to **–16dB filter gain** : +7.9 dBm (vxtd = 0xff) > **tel. line level** > -40.1 dBm (vxtd = 0x01)
R95 adjusted to **0 dB filter gain** : - 8.1dBm (vxtd = 0xff) > **tel. line level** > -56.1 dBm (vxtd = 0x01)
R95 adjusted to **+ 6dB filter gain** : -14.1dBm (vxtd = 0xff) > **tel. line level** > -62.1 dBm (vxtd = 0x01)
@ when level Rx_tfork_*mx*_in of 3.3 dBm corresponds to telephone line level –6 dBm.

**Vox attack time** (tva of VTD) : $1.5 * 10^{-3}$ s < Vox attack time < $35 * 10^{-3}$ s

Minimal attack time tva_min = $1.5 * 10^{-3}$ s @ VXSI = 0xff = 255 , host => 0x00.
Maximal attack time tva_max = $35 * 10^{-3}$ s @ VXSI = 0x19 = 25 , host => 0xff.
Embedded PAS 2000 software conversion in C language :

VXSI = 255 – ( Host value / 255) * 230

**Vox decay time** (tvd) :

Minimal : Hardware dictated (VTD) ; between 0.20 s (min) and 0.46 s (max).
Maximal : PAS2000 embedded software determined.
(software vdo_ptt_ra has to take over the hardware Vox threshold detect (VTD) within 0.20 seconds.)

# 8. VOX AND TELEPHONE HYBRID PROPERTIES .

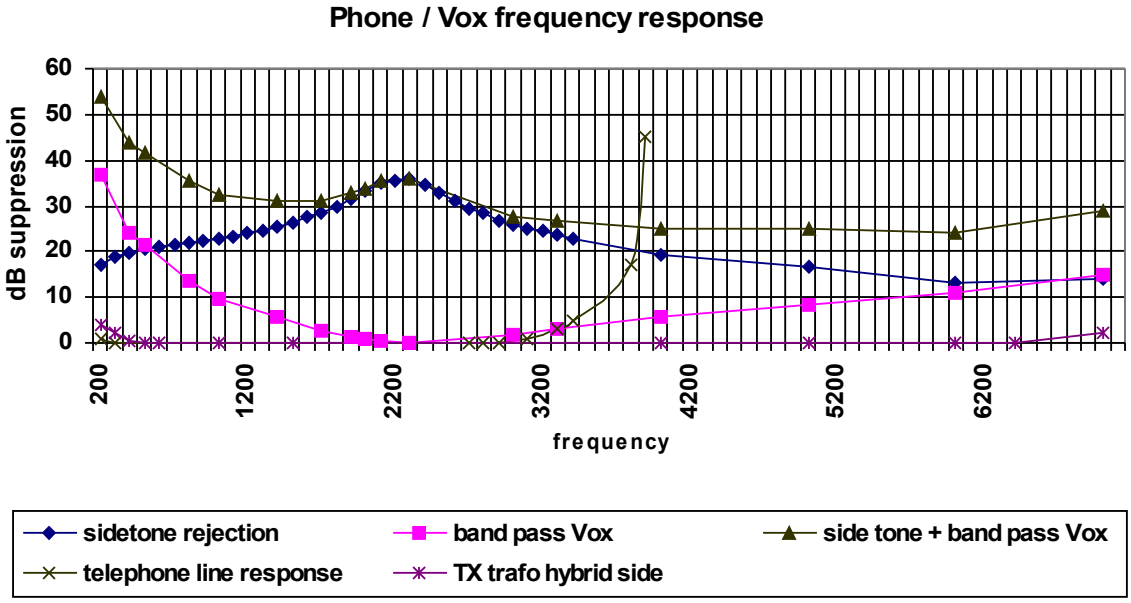



**figure and table representing suppression versus frequency of telphone hybrid and Vox pre filter.**

| Freq. KHz | Sidetone Rejection +dB | Vox bandpass +dB | Sidetone + Bandpass +dB |
|---|---|---|---|
| **0.2** | 17.0 | 36.9 | 53.9 |
| **0.3** | 18.7 | | |
| **0.4** | 19.7 | 23.9 | 43.6 |
| **0.5** | 20.4 | 21.4 | 41.8 |
| **0.6** | 21.0 | | |
| **0.7** | 21.4 | | |
| **0.8** | 21.7 | 13.6 | 35.3 |
| **0.9** | 22.3 | | |
| **1.0** | 22.7 | 9.8 | 32.5 |
| **1.1** | 23.2 | | |
| **1.2** | 24.0 | | |
| **1.3** | 24.7 | | |
| **1.4** | 25.4 | 5.8 | 31.2 |
| **1.5** | 26.4 | | |
| **1.6** | 27.5 | | |
| **1.7** | 28.5 | 2.8 | 31.3 |
| **1.8** | 29.8 | | |
| **1.9** | 31.4 | 1.4 | 32.8 |
| | | | |

| Freq. KHz | Sidetone Rejection +dB | Vox Bandpass +dB | Sidetone + Bandpass +dB |
|---|---|---|---|
| **2.0** | 33.2 | 0.7 | 33.7 |
| **2.1** | 35.0 | 0.6 | 35.6 |
| **2.2** | 35.5 | | |
| **2.3** | 36.1 | 0 | 36.1 |
| **2.4** | 34.8 | | |
| **2.5** | 32.8 | | |
| **2.6** | 31.1 | | |
| **2.7** | 29.4 | | |
| **2.8** | 28.4 | | |
| **2.9** | 26.8 | | |
| **3.0** | 25.8 | 1.6 | 27.4 |
| **3.1** | 25.1 | | |
| **3.2** | 24.4 | | |
| **3.3** | 23.6 | 2.9 | 26.5 |
| **3.4** | 22.7 | | |
| **4.0** | 19.3 | 5.6 | 24.9 |
| **5.0** | 16.6 | 8.4 | 25.0 |
| **6.0** | 13.2 | 11.0 | 24.2 |
| **7.0** | 14.2 | 14.7 | 28.9 |

**Explanation suppression table Telephone hybrid and Vox pre filter :**

The measured values in the table are collected under the following circumstances :

- The PAS2000 telephone hybrid is connected to the SIEMENS H150E office point home central via 20 meters of twisted pair cat.5 STP cable.
- A sinus signal coming from a MARCONI 2945 communication service monitor, is brought in on the Mobile input of the Pas2000. This signal is routed via the Matrix to the PSTN output on to the Telephone line . The PSTN RX signal is picked up by the PAS2000 telephone hybrid , and routed via the matrix to the Mobile output. The Mobile output is connected to the input of the MARCONI measuring the response.
- The Hybrid is adjusted to exhibit maximum sidetone rejection according to procedure.

**The Table is representing the following items :**

- **Sidetone rejection = Column 2 :** sidetone suppression is defined as ratio hybride RX level when Hybrid places a signal on the telephone line and the hybrid RX signal when the same telephone line level is established by an external source. This suppression is measured in the following way ; The response To a PSTN TX on PSTN RX is measured with the MARCONI on the Mobile output. This response, which is balanced by a matched simulated telephone line impedance on a differential amplifier, in the hybrid is called 'Urxb' . Then the path of the matched simulated telephone impedance is silenced inside the telephone hybrid by short circuiting C19 and the RX response ( called 'Urx' ) is measured again. The sidetone rejection with the telephone line as reference ,is calculated by the formula : Sidetone_rejection = Urx – Urxb – Trafo_loss_RX – Trafo_loss_TX in which Urx – Urxb is the rejection with the primary (hybrid) side of the trafo as reference.
- **Vox band pass suppression = column 3 :** Suppression of Vox prefilter with 2.2KHz centre frequency. Suppression = 1/gain. This is a second order filter. The signal offered to the signal detecting circuit of the Vox is first passing the filter.
- **Sidetone rejection + Vox Band pass filter suppression = column 4 :** This is the frequency response of the signal offered to the Vox with respect to the signal on the telephone line placed by the PAS2000 hybrid. Reference suppression is 0dB at 2200 KHz when external source places similar telephone line level.

**VOICE SWITCH OPERATION.**

**Principle** :When a matrix connection has been built between the radio and a telephone line, the Push to talk switch for the radio on the PAS2000 is activated by the received RX telephone line signal .

**PTT radio algorithm :** PTT_radion_ctrl = ( VTD and ENVOX_Ran) or (VDO_PTT_Ran)

| | | |
|---|---|---|
| VTD | = | hardware driven Vox threshold detect. |
| ENVOX_RAN | = | enable signal for VTD. |
| VDO_PTT_Ran | = | software driven control signal |

ENVOX_Ran (Enable hardware Vox detect) is set by software as soon as a connection between radio_n and the telephone line has been established. When a received (RX) signal on the telephone line exceeds a threshold level, it triggers hardware signal VTD which becomes active = high. When ENVOX_Ran is high the PTT_radion_ctrl is becoming immediately active. The minimal 200msec on-time of VTD is giving the processor, time to take over with VDO_PTT, This VDO_PTT__Ran is set by software when the hardware generated Vox Threshold detect = VTD is **polled** 'high' , and stays high until a decay time has been counted out

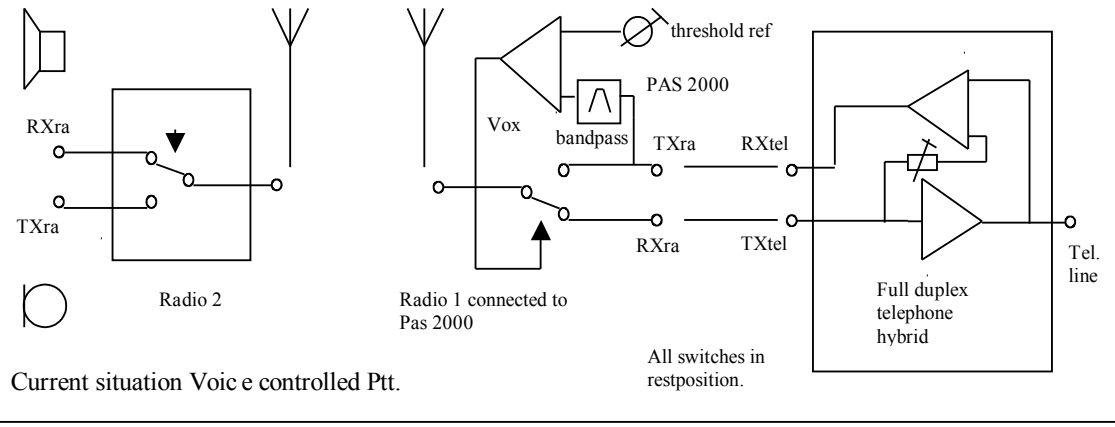
since the last high to low transistion of VTD. The hardware generated VTD in the PTT radio control algorithm guarantees fast attack times where software control would lead to larger response (attack) time.

**Limitations : W**hen the radio where the PAS2000 radio is communicating with, starts transmitting it can happen that the PTT for the radio on the PAS 2000 also is activated by the Vox. With the sense input of the telephone Voice switch on the RX side of the PAS2000 telephone hybrid, this occurs when the Hybrid TX is sending a signal on the telephone line while it is in the mean time picked up by this RX side. This is caused by insufficient sidetone rejection of the full duplex telephone hybrid. Since the radio communication is semi duplex (when it transmits it can not receive and visa versa ) it looses the Vox threshold exceeding transmitted radio signal from the other side, when the pas radio also switches to transmission. Eventually the PAS 2000 radio will fall back to receiving and the cycle can start again. The following modifications in PAS2000_HFR_0015 , _0024, _0025 were executed to eliminate this problem:

a) 0015 : The Telephone hybrid sidetone rejection has been improved , resulting in the properties presented in the table.

b) 0024 : The Vox pre filter is given a small band pass shape property with the centre frequency at which the telephone hybrid has the maximum sidetone rejection. (because it is adjusted at this frequency.)

c) 0025 : The output level of the TX transmitting amplifier in the telephone hybrid is limited with a soft clipper in such a way that it limits the level being placed on the telephone line to a maximum of –6 dBm on this telephone line.



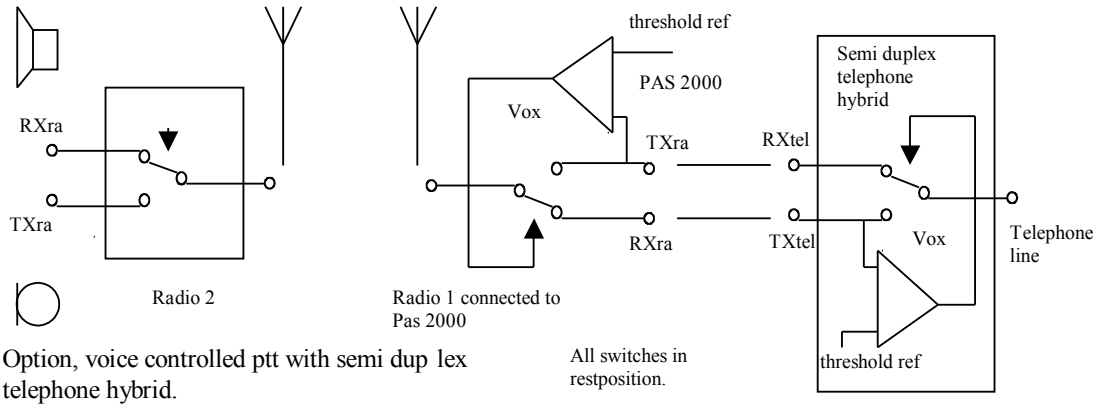

Current situation Voic e controlled Ptt.

To achieve complete assurance in proper radio PTT control by the VOX ,when the above mentioned measures are not probate, there are several options. Two of them are mentioned :

**1) Use of the full duplex telephone hybrid in combination with Two extra Vox switches** , one on radio1 RX and one on radio 2 RX. The PAS2000 may only generate a radio PTT by the telephone VOX when the radio RX Vox is not active .The algorithm for radio control by the PAS2000 will then become :

PTT_radion_ctrl = ( VTD and ENVOX_Ran and not ( radion_RX_vox_detect ) ) or
( VDO_PTT_Ran and not ( radion_RX_vox_detect ) )

**2) Replacement of the full duplex telepone hybrid by a semi duplex one with a built in Vox.**




Option, voice controlled ptt with semi dup lex telephone hybrid.

All switches in restposition.

# 9. SETTINGS AND ADJUSTMENT PROCEDURES

## 9.1 Adjusting the Sidetone rejection to get maximum suppression.

**Objective :** Matching the simulated telephone line impedance of the PAS2000 hybrid with the connected telephone line. The Hybrid (PSTN interface PCB) which can be adjusted to change the phase and the gain of the simulated telephone line , to achieve this goal. These potentiometers are :

- Gain potentiometer , R57 (adjusted at 2.2 KHz).
- Negative phase shift potentiometer R48 adjusted at 2.2KHz , simulating line capacitance.
- Positive phase shift potentiometer R41, adjusted at 300 Hz, simulating line and transformer inductance.

There are Three test points on the PSTN interface PCB for monitoring during adjustment.

- TP1 : representing the received telephone line level.
- TP2 : representing the level on the simulated telephone level.
- TP3 : The telephone RX signal with sidetone rejection. Actual the differential of the two signals TP1 and TP2.

**Adjustment procedure :**

1. Place the Probe of channel A Of a 2 channel oscilloscope on test point TP1 of the PAS2000 telephone hybrid. Place the Probe of channel B on TP2. Adjust both channels of the scoop to the same settings.
2. Connect a sinus signal generator to one of the inputs of the PAS2000 and route this input with the matrix to the PAS2000 PSTN output. Connect a milli volt /dBu meter to one of the PAS2000 outputs and route the PSTN input to this output. ( you can also use TP3 to connect the milli volt meter.)
3. Connect the PAS2000 with the telephone line, by calling another telephone unit. Take care that during the procedure this telephone can not pick up noise since this disturbs the adjustment. If possible mute the microphone of this telephone.
4. Bring a 2.2 KHz sinus signal via the matrix of the pas2000 on the telephone line resulting in a nominal level of –12dBm.
5. Adjust R57 (amplitude of sinus on channel B) and R48 ( negative phase angle of sinus on channel B ) so that the sinus waves on both scoop channels are falling exactly together (in phase with equal amplitudes). Fine tune to a minimum level on the milli volt meter.
6. Alter the sinus signal frequency into 300 Hz.
7. Adjust R48 ( positive phase angle of sinus on channel B ) so that the sinus waves on both scoop channels are falling exactly together (in phase with equal amplitudes). Fine tune to a minimum level on the milli voltmeter.
8. Set the sinus generator back to 2.2 KHz and repeat step 3, 4 and 5.
9. Ready.

## 9.2 Operator speaker output setting

With jumper settings the operator speaker output can be configured in two different ways :

1. **Transformer output :** with output impedance of 600Ω , unloaded output level ,nominal +8dBm / Maximal +14dBm . **Jumper setting:** J13, J14, J15, J21 in the 2-3 position.
2. **Bridged Amplifier output :** Output power 1.0 Watt in 8Ω , ( 0.3 % typ THD @ 0.3.Watt) , (each output 6 Volt DC biassed with respect to +12V power GND ). . The overall gain of the amplifier with input between J21,2 and J15,2 (output of transformer of configuration 1 ) can be adjusted with R282 between +7.6 dB and -∞ . **Jumper setting:** J13, J14, J15, J21 in the 1-2 position.

# 10. TECHNICAL SPECIFICATIONS

## 10.1 General specifications :

| | | |
|---|---|---|
| Supply voltage | : | 12 Volt. |
| Current Consumption | : | 500 mA continuous , 1300 mA peak (Power amp in 8 Ω ) |
| Fuse | : | 1000 mA / T (slow) |

## 10.2 Audio Performance :

**Audio Path : Audio input => Audio output (except PSTN and operator power amplifier)**
Audio inputs and outputs are galvanic isolated by an audio transformer.

| | | |
|---|---|---|
| Conditions | : | Audio output trafo terminated with 600Ω load. |
| Audio output impedance | : | 600Ω (galvanic separated by transformer ) |
| Audio input impedance | : | 600Ω (galvanic separated by transformer ) |
| Frequency response | : | 135 Hz – 5.0 KHz (-3dB) |
| Nominal output level | : | + 4 dBm (* Distortion <= 0.1% @ 1KHz) |
| Maximal output level | : | + 9 dBm (* Distortion <= 1.0 % @ 1KHz) |

| Nominal Input level | : | + 4 | - 5 | - 14 | - 23 | - 32 | dBm |
|---|---|---|---|---|---|---|---|
| Input gain @ | : | 0 | + 9 | + 18 | + 27 | + 36 | dB |

| | | |
|---|---|---|
| Maximum input level | : | 6 dB above nominal. |
| **Operator power amp.** | **:** | **Bridged Amplifier output .** |
| Output power in 8 Ω | : | 2.5 Watt Peak ( over whole temperature range 0 – 55°C ) |
| | : | 80 mW continuous at 55°C ambient. |
| | | 150 mW continuous at 25°C ambient |
| THD | : | 0.3% @ 0.5 Watt |
| DC offset both outputs | : | 6 Volt DC biassed with respect to +12V power GND. |
| Protection | : | Short circuit and Thermal protected. |
| Supply | : | amplifier supplied by the fused external +power = +12 Volt. |

** Distortion defined as:* $distortion = \frac{n+d}{s+n+d} * 100\% = \frac{V2}{V1} * 100\%$

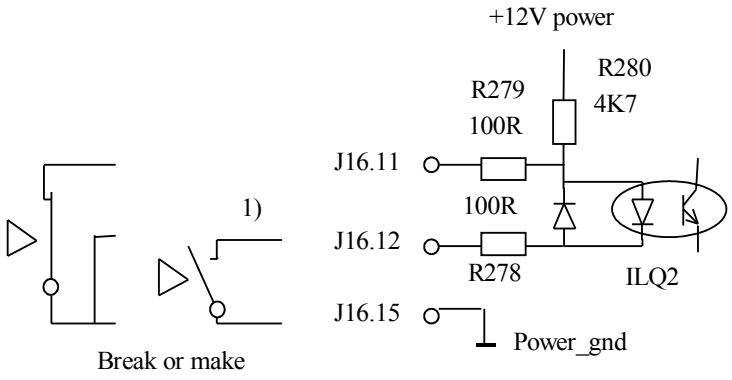
*with V2 = voltage level measurement with 1 KHz notch, V1 = voltage level measurement without notch.*
*n = noise amplitude, s = 1 KHz signal amplitude , d = distortion amplitude.*

## 10.3 Control performance

| Symbol | | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Iptt_ra1,2 | Output | Push To talk Radio_1,2 opto. ( CTRmin = 100 % ) | 1.6 | - | - | mA |
| Vptt_ra1,2 | Output | Ptt Radio 1,2 opto Voltage range. | 0 | - | 30.0 | Volt |
| Isqi | Output | Squelch indication opto. ( CTRmin = 50 % ) | 550 | - | - | µA |
| Vsqi | Output | Squelch indication output voltage range | 0 | | 30.0 | Volt |
| Ippto | Input | Push to talk operator . ( CTRmin = 100 % ) | 0.16 | - | 2.3[1)] | mA |
| Vuo | Input | Ptt operator voltage range across J16,11 and J16,15or J16,12 and J16,15 voltages with respect to power ground. | 0 | | 12.0 | Volt |
| Iuo | Output | User outputs. ( CTRmin = 100 % ) | 1.6 | - | - | mA |
| Uuo | Output | User output Voltage range | 0 | - | 30.0 | Volt |
| Iui | Input | User Inputs. (Uui = 1.32 Volt , CTRmin = 50 % ) | 100 | - | - | µA |
| Vui | Input | User input Voltage range. (100µA – 13.2mA) | 1.32 | - | 30.0 | Volt |

All above control I/O isolated by opto couplers ( Siemens Quad ILQ-2).

1) Internal The PAS2000 the anode of the optocoupler diode is connected via a series resistor of 4K7 with the +power which is the fused +12 volt external Unit power. PTT operator activated by closed switch contact between J16 pin 12 (cathode via series resistor of 100Ω) and J16 pin 15 (power GND).




PTT operator connection

# 11. I/O CONNECTOR PIN CONFIGURATION

| Logging recorder interface (con.1) | | |
|---|---|---|
| 9 pins female sub d | | |
| **Pin nmbr** | **description** | **acronym** |
| 1 (in) | Play back 1+ | PB1+ |
| 2 (in) | Play back 1- | PB1- |
| 3 (out) | Recording 1+ | REC1+ |
| 4 (out) | Recording 1 - | REC1- |
| 5 | | |
| 6 (in) | Play back 2+ | PB2+ |
| 7 (in) | Play back 2- | PB2- |
| 8 (out) | Recording 2+ | REC2+ |
| 9 (out) | Recording 2 - | REC2- |
| *10* | *House = Gnd_mech* | |

| Radio RD40 interface (J11 and J12) | | |
|---|---|---|
| 9 pins female sub d | | |
| **Pin nmbr** | **description** | **acronym** |
| 1 (out) | Radio_mic_in+ | |
| 2 (out) | Radio_mic_in- | |
| 3 | | |
| 4 | | |
| 5 | | |
| 6 (out) | Radio Ptt opto + | |
| 7 (out) | Radio Ptt opto - | |
| 8 (in) | Radio_LS_out+ | |
| 9 (in) | Radio_LS_out- | |
| *10* | *House = Gnd_mech* | |

| Operator interface (J16) | | |
|---|---|---|
| 15 pins female sub d | | |
| **Pin nmbr** | **Description** | **acronym** |
| 1 | + power | |
| 2 | | |
| 3 (in) | Operator Mic + | |
| 4 (in) | Operator Mic - | |
| 5 (out) | Sqi opto + | |
| 6 (out) | Sqi opto - | |
| 7 | Power gnd | |
| 8 | Power gnd | |
| 9 | + Power | |
| 10 | | |
| 11 (in) | Operator PTT opto + | |
| 12 (in) | Operator PTT opto - | |
| 13 (out) | Operator speaker + | |
| 14 (out) | Operator speaker - | |
| 15 | Power gnd | |
| *16* | *House = Gnd_mech* | |

| PC rs232 interface (J3) | | |
|---|---|---|
| 9 pins male sub d | | |
| **Pin nmbr** | **description** | **acronym** |
| 1 | n.c. | |
| 2 (out) | Transmit | TXD |
| 3 (in) | Receive | RXD |
| 4 | n.c. | |
| 5 | Separated GND Return for Tx and Rx | GND_ser |
| 6 | n.c. | |
| 7 | Mechanical Gnd | Gnd_mech |
| 8 | n.c. | |
| 9 | n.c. | |
| *10* | *House = Gnd_mech* | |

| Flash programming interface (J2) | | |
|---|---|---|
| 8 pins RJ 45 | | |
| **Pin nmbr** | **description** | **acronym** |
| 1 (out) | Data output | Miso |
| 2 (in) | Instruction input | Mosi |
| 3 (in) | Clock in | Sck |
| 4 | n.c. | |
| 5 | Pas2000 internal Gnd | GND_D |
| 6 (in) | '+5V' = downloading | |
| 7 | n.c. | |
| 8 (out) | +5 Volt | |
| | | |

**Remarks :**
'In' and 'Out' referred to the PAS2000.
n.c. = not connected.

**PC RS232 interfac**e TXD and RXD are optical isolated (Siemens SFH 618) from the in- and ex-ternal power, whereas the RS232 +/- 12 Volt supply also is separated.
**Flash programming in/output**s are **not** isolated but proteced by 1 K series resistors and diode clamps.

# 12. PAS2000 EMBEDDED SOFTWARE DIRECTIVES.

1. Do not use setting CPOL = 0 but Setting CPOL = 1 and adapt the SSBUS clock circuit. see also PAS2000_HFR_0007.

2. DAC08 pinning : Pin 9 = B1 = MSB and Pin 16 = B8 = LSB.

3. Data Shifting (transmission of bytes via the SPI bus) on the SSB is only allowed when **none** of the latch signals is active to avoid data being placed into the wrong shifregisters. ( ELP= active High, LEO# = active low, LEI = active high ). Wait after an ELP reset strobe, minimal 5 * 100 K * 2.2 N = 1.1 milli seconds to give ZCLE_SSB_n the time to generate the safety latch strobe, before transmitting the next byte train out of Mosi into the shift registers

4. Load potentiometer control bytes immediately after reset in INIT() with 0x00 (full Mute) , and set the matrix switch control bits ( 0 = off) .

5. The diagonal matrix switches must be set permanently in the off position in the user version of the Host software.

6. Use for (re)setting a processor output pin an intermediate variable. Do inquiry of this pin not directly on this pin ( since we then get the electrical level translated into a 1 or 0 ) but on the intermediate variable unless the electrical status ( expressed in 1 or 0 ) must be known by the program!

7. Make use of software debouncing in program parts which are inquiring the status of switches or opto coupler inputs

8. In order to prevent the radio transmitters to be switched on during poweron, RESET immediately after processor_reset ( first lines in INIT() ), ENVOX_RA1 = P3_4, ENVOX_RA2 = P3_6, VDO_PTT_RA1 = P3_5 and VDO_PTT_RA2 = P3_7.

9. The PAS2000 has an telephone hybrid with sidetone rejection . This means that the telephone signal which is received by the telephone interface of the PAS, first undergoes a subtraction by the telephone signal which is transmitted by the PAS before it is passed through to the matrix. Therefore it is necessary to match the impedance of the simulated telephone line in the signal comparing sidetone circuit with the impedance of the telephone line. When this matching is poorly, unit feedback can occur via the following loop : operator microphone => PSTN transmission => PSTN reception => (poorly) suppression => operator speaker => (acoustic feedback ) => operator microphone. This feedback can be reduced by lowering the gain of the mentioned loop. The following measures can be taken to prevent the telephone interface from howling by feedback when the PSTN in- out-put matrix points and also the operator speaker and operator microphone are set . Poor sidetone rejection causes also the Vox to become activated when a signal is transmitted by the PAS2000 PSTN TX itself.

a) Take care of proper sidetone adjustment of telephone hybrid.

b) When the telephone line is disconnected while the The PSTN input is still routed to the operator speaker and the operator microphone is routed to the PSTN output and Out-put then unit feedback becomes possible because of poor sidetone suppression by bad impedance matching in the telephone hybrid. Therefore ‘’AND’’ the Matrix points for PST-in and Out-put with the telephone OF_HOOK variable. The telephone procedure then becomes ; when making a call first take the telephone hybrid off hook, then enable the PSTN in-output matrix points. When terminating a call first disable the telephone matrix in- out-put points then place the hybrid on hook.

c) In case the telephone is connected with the operator, mute the operator spkr potmeter or the telephone_RX input gain adjustable pre amplifier when the operator microphone PTT switch is pressed.

**VOX operation :**

ENVOX_Ran (Enable hardware Vox detect) is set by software as soon as a connection between radio_n and the telephone line has been established. VDO_PTT__Ran is set by software when the hardware generated telephone Vox Threshold detect = VTD is polled 'high' , and stays high until a decay time has been counted out since the last high to low transistion of VTD.

# 13. SERIAL SHIFT REGISTER CHAIN 1 FOR OUTPUT

| BYTE NUMBER 24 / latch pulse ZCLE1_SSB | | | BYTE NUMBER 23 / latch pulse ZCLE2_SSB | | |
|---|---|---|---|---|---|
| Matrix | 4094 IC50 mb | 4053 IC | Matrix | 4094 IC49 mb | 4053 IC |
| Dedication | Matrix switches 1_1 - 6_1 | | Dedication | Matrix switches 1_2 - 6_2 | |
| serial in from | SERDATO_SSB µp P1_5 | | serial in from | 4094 IC 50 mb | PIN 10 |
| column_row | 4094 pin nr | 4053 ic,pin nr | column_row | 4094 pin nr | 4053 ic,pin nr |
| MS11 | pin 4 lsb | mb 33,10 | MS12 | pin 4 lsb | mb 33,11 |
| MS21 | 5 | mb 31,10 | MS22 | 5 | mb 31,11 |
| MS31 | 6 | mb 29,10 | MS32 | 6 | mb 29,11 |
| MS41 | 7 | mb 27,10 | MS42 | 7 | mb 27,11 |
| MS51 | 14 | mb 25,10 | MS52 | 14 | mb 25,11 |
| MS61 | 13 | mb 23,10 | MS62 | 13 | mb 23,11 |
| T1UO1 | 12 | - | T1UO3 | 12 | - |
| T1UO2 | 11 | - | T1UO4 | 11 | - |

Matrix Switch control bit MS nn = 1 Switch = on , MS nn = 0 switch = off.

| BYTE NUMBER 22 / latch pulse ZCLE3_SSB | | | BYTE NUMBER 21 / latch_pulse ZCLE4_SSB | | |
|---|---|---|---|---|---|
| Matrix | 4094 IC48 mb | 4053 IC | Matrix | 4094 IC47 mb | 4053 IC |
| Dedication | Matrix switches 1_3 - 6_3 | | Dedication | Matrix switches 1_4 - 6_4 | |
| serial in from | 4094 IC 49 mb PIN 10 | | serial in from | 4094 IC 48 mb | PIN 10 |
| column_row | 4094 pin nr | 4053 ic,pin nr | column_row | 4094 pin nr | 4053 ic,pin nr |
| MS13 | pin 4 lsb | mb 33,9 | MS16 | pin 4 lsb | mb 32,10 |
| MS23 | 5 | mb 31,9 | MS26 | 5 | mb 30,10 |
| MS33 | 6 | mb 29,9 | MS36 | 6 | mb 28,10 |
| MS43 | 7 | mb 27,9 | MS46 | 7 | mb 26,10 |
| MS53 | 14 | mb 25,9 | MS56 | 14 | mb 24,10 |
| MS63 | 13 | mb 23,9 | MS66 | 13 | mb 22,10 |
| T1UO5 | 12 | - | T1UO7 | 12 | - |
| T1UO6 | 11 | - | T1UO8 | 11 | - |

| BYTE NUMBER 20 / latch pulse ZCLE5_SSB | | | BYTE NUMBER 19 / latch_pulse ZCLE6_SSB | | |
|---|---|---|---|---|---|
| Matrix | 4094 IC46 mb | 4053 IC | Matrix | 4094 IC45 mb | 4053 IC |
| Dedication | Matrix switches 1_5 - 6_5 | | Dedication | Matrix switches 1_6 - 6_6 | |
| serial in from | 4094 IC 47 mb PIN 10 | | serial in from | 4094 IC 46 mb | PIN 10 |
| column_row | 4094 pin nr | 4053 ic,pin nr | column_row | 4094 pin nr | 4053 ic,pin nr |
| MS15 | pin 4 lsb | mb 32,11 | MS14 | pin 4 lsb | mb 32,9 |
| MS25 | 5 | mb 30,11 | MS24 | 5 | mb 30,9 |
| MS35 | 6 | mb 28,11 | MS34 | 6 | mb 28,9 |
| MS45 | 7 | mb 26,11 | MS44 | 7 | mb 26,9 |
| MS55 | 14 | mb 24,11 | MS54 | 14 | mb 24,9 |
| MS65 | 13 | mb 22,11 | MS64 | 13 | mb 22,9 |
| T1UO9 | 12 | - | T1UO11 | 12 | - |
| T1UO10 | 11 | - | T1UO12 | 11 | - |

| BYTE NUMBER 18 / latch pulse ZCLE1_SSB | | | BYTE NUMBER 17 / latch_pulse ai IC 7,11 | | |
|---|---|---|---|---|---|
| Potmeter Y1 | 4094 IC 9 ai1 | DAC08 | Potmeter X1 | 4094 IC 8 ai1 | DAC08 IC |
| Dedication | play back 1 attenuation control | | Dedication | recorder 1 attenuation control | |
| serial in from | mb 4094 IC 45 pin 10 | | serial in from | ai1 4094 IC 9 pin 10 | |
| Bit description | 4094 pin nr | DAC08 ic,pin | Bit description | 4094 pin nr | DAC 08 ic,pin |
| PY11 | pin 4 lsb | ai111-12, 9msb | PX11 | pin 4 lsb | ai1 3-6, 9msb |
| PY12 | 5 | ai1 11-12,10 | PX12 | 5 | ai1 3-6,10 |
| PY13 | 6 | ai1 11-12,11 | PX13 | 6 | ai1 3-6,11 |
| PY14 | 7 | ai1 11-12,12 | PX14 | 7 | ai1 3-6,12 |
| PY15 | 14 | ai1 11-12,13 | PX15 | 14 | ai1 3-6,13 |
| PY16 | 13 | ai1 11-12,14 | PX16 | 13 | ai1 3-6,14 |
| PY17 | 12 | ai1 11-12,15 | PX17 | 12 | ai1 3-6,15 |
| PY18 | 11 | ai1 11-12,16 | PX18 | 11 | ai1 3-6,16 |

| BYTE NUMBER 16 / latch pulse ic 19,11 ai1 | | | BYTE NUMBER 15 / latch_pulse ZCLE2_SSB | | |
|---|---|---|---|---|---|
| Potmeter X2 | 4094 IC 20 ai1 | DAC08 | gain ctrl Y2 | 4094 IC 13 ai1 | 4053 IC 14 ai1 |
| Dedication | recorder 2 attenuation control | | Dedication | play back 2 gain control | |
| serial in from | ai1 4094 IC 8 pin 10 | | serial in from | ai1 4094 IC20 pin 10 | |
| Bit description | 4094 pin nr | DAC08 ic,pin | Bit description | 4094 pin nr | 4053 ic,pin |
| PX21 | pin 4 lsb | ai115-18, 9msb | ISY20 | pin 4 lsb | ai1 14,9 lsb |
| PX22 | 5 | ai1 15-18,10 | ISY21 | 5 | ai1 14,11 |
| PX23 | 6 | ai1 15-18,11 | IS22 | 6 | ai1 14,10 |
| PX24 | 7 | ai1 15-18,12 | ISY23 | 7 | ai1 14,6 |
| PX25 | 14 | ai1 15-18,13 | - | 14 | - |
| PX26 | 13 | ai1 15-18,14 | - | 13 | - |
| PX27 | 12 | ai1 15-18,15 | - | 12 | - |
| PX28 | 11 | ai1 15-18,16 | - | 11 | - |

Potmeter control byte PX nn or PY nn = 0xff = full volume. PX nn or PY nn = 0x00 = mute .

| BYTE NUMBER 14 / latch pulse ZCLE1_SSB | | | BYTE NUMBER 13 / latch_pulse ZCLE2_SSB | | |
|---|---|---|---|---|---|
| gain ctrl Y1 | 4094 IC 1 ai1 | 4053 IC 2 ai1 | Potmeter Y2 | 4094 IC 21 ai1 | DAC 08 |
| Dedication | play back 1 gain control | | Dedication | play back 2 attenuation control | |
| serial in from | ai1 4094 IC 13 pin 10 | | serial in from | ai1 4094 IC1 pin 10 | |
| Bit description | 4094 pin nr | 4053 ic,pin | Bit description | 4094 pin nr | DAC 08 ic,pin |
| ISY10 | pin 4 lsb | ai1 2,9 lsb | PY21 | pin 4 lsb | ai123-24, 9msb |
| ISY11 | 5 | ai1 2,11 | PY22 | 5 | ai1 23-24,10 |
| ISY12 | 6 | ai1 2,10 | PY23 | 6 | ai1 23-24,11 |
| ISY13 | 7 | ai1 2,6 | PY24 | 7 | ai1 23-24,12 |
| - | 14 | - | PY25 | 14 | ai1 23-24,13 |
| - | 13 | - | PY26 | 13 | ai1 23-24,14 |
| - | 12 | - | PY27 | 12 | ai1 23-24,15 |
| - | 11 | - | PY28 | 11 | ai1 23-24,16 |

| BYTE NUMBER 12 / latch pulse ZCLE3_SSB | | | BYTE NUMBER 11 / latch_pulse ai2 IC 7,11 | | |
|---|---|---|---|---|---|
| Potmeter Y3 | 4094 IC 9 ai2 | DAC08 | Potmeter X3 | 4094 IC 8 ai2 | DAC08 |
| Dedication | RX Radio1 attenuation control | | Dedication | TX radio 1 attenuation control | |
| serial in from | ai1 4094 IC 21 pin 10 | | serial in from | ai2 4094 IC 9 pin 10 | |
| Bit description | 4094 pin nr | DAC08 ic,pin | Bit description | 4094 pin nr | DAC 08 ic,pin |
| PY31 | pin 4 lsb | ai2 11-12,9msb | PX31 | pin 4 lsb | ai2 3-6, 9 msb |
| PY32 | 5 | ai2 11-12,10 | PX32 | 5 | ai2 3-6,10 |
| PY33 | 6 | ai2 11-12,11 | PX33 | 6 | ai2 3-6,11 |
| PY34 | 7 | ai2 11-12,12 | PX34 | 7 | ai2 3-6,12 |
| PY35 | 14 | ai2 11-12,13 | PX35 | 14 | ai2 3-6,13 |
| PY36 | 13 | ai2 11-12,14 | PX36 | 13 | ai2 3-6,14 |
| PY37 | 12 | ai2 11-12,15 | PX37 | 12 | ai2 3-6,15 |
| PY38 | 11 | ai2 11-12,16 | PX38 | 11 | ai2 3-6,16 |

| BYTE NUMBER 10 / latch pulse ic 19,11 ai2 | | | BYTE NUMBER 9 / latch_pulse ZCLE4_SSB | | |
|---|---|---|---|---|---|
| Potmeter X4 | 4094 IC 20 ai2 | DAC08 | gain ctrl Y4 | 4094 IC 13 ai2 | 4053 IC 14 ai2 |
| Dedication | TX radio 2 attenuation control | | Dedication | : RX radio 2 gain control | |
| serial in from | ai2 4094 IC 8 pin 10 | | serial in from | : ai2 4094 IC20 pin 10 | |
| Bit description | 4094 pin nr | DAC08 ic,pin | Bit description | 4094 pin nr | 4053 ic,pin |
| PX41 | pin 4 lsb | ai215-18, 9msb | ISY40 | pin 4 lsb | ai2 14,9 lsb |
| PX42 | 5 | ai2 15-18,10 | ISY41 | 5 | ai2 14,11 |
| PX43 | 6 | ai2 15-18,11 | ISY42 | 6 | ai2 14,10 |
| PX44 | 7 | ai2 15-18,12 | ISY43 | 7 | ai2 14,6 |
| PX45 | 14 | ai2 15-18,13 | - | 14 | - |
| PX46 | 13 | ai2 15-18,14 | - | 13 | - |
| PX47 | 12 | ai2 15-18,15 | - | 12 | - |
| PX48 | 11 | ai2 15-18,16 | - | 11 | - |

| BYTE NUMBER 8 / latch pulse ZCLE1_SSB | | | BYTE NUMBER 7 / latch_pulse ZCLE2_SSB | | |
|---|---|---|---|---|---|
| gain ctrl Y3 | 4094 IC 1 ai2 | 4053 IC 2 ai2 | Potmeter Y4 | 4094 IC 21 ai2 | DAC 08 |
| Dedication | RX RADIO 1 gain control | | Dedication | RX RADIO 2 attenuation control | |
| serial in from | ai2 4094 IC 13 pin 10 | | serial in from | ai2 4094 IC1 pin 10 | |
| Bit description | 4094 pin nr | 4053 ic,pin | Bit description | 4094 pin nr | DAC 08 ic,pin |
| ISY30 | pin 4 lsb | ai2 2,9 lsb | PY41 | pin 4 lsb | ai2 23-24, 9msb |
| ISY31 | 5 | ai2 2,11 | PY42 | 5 | ai2 23-24,10 |
| ISY32 | 6 | ai2 2,10 | PY43 | 6 | ai2 23-24,11 |
| ISY33 | 7 | ai2 2,6 | PY44 | 7 | ai2 23-24,12 |
| - | 14 | - | PY45 | 14 | ai2 23-24,13 |
| - | 13 | - | PY46 | 13 | ai2 23-24,14 |
| - | 12 | - | PY47 | 12 | ai2 23-24,15 |
| - | 11 | - | PY48 | 11 | ai2 23-24,16 |

| BYTE NUMBER 6 / latch pulse ZCLE5_SSB | | | BYTE NUMBER 5 / latch_pulse ai3 IC 7,11 | | |
|---|---|---|---|---|---|
| Potmeter Y5 | 4094 IC 9 ai2 | DAC08 | Potmeter X5 | 4094 IC 8 ai3 | DAC08 IC |
| Dedication | Mic operator attenuation control | | Dedication | LS operator attenuation control | |
| serial in from | ai3 4094 IC 21 pin 10 | | serial in from | ai3 4094 IC 9 pin 10 | |
| Bit description | 4094 pin nr | DAC08 ic,pin | Bit description | 4094 pin nr | DAC 08 ic,pin |
| PY51 | pin 4 lsb | ai3 11-12, 9msb | PX51 | pin 4 lsb | ai3 3-6, 9 msb |
| PY52 | 5 | ai3 11-12,10 | PX52 | 5 | ai3 3-6,10 |
| PY53 | 6 | ai3 11-12,11 | PX53 | 6 | ai3 3-6,11 |
| PY54 | 7 | ai3 11-12,12 | PX54 | 7 | ai3 3-6,12 |
| PY55 | 14 | ai3 11-12,13 | PX55 | 14 | ai3 3-6,13 |
| PY56 | 13 | ai3 11-12,14 | PX56 | 13 | ai3 3-6,14 |
| PY57 | 12 | ai3 11-12,15 | PX57 | 12 | ai3 3-6,15 |
| PY58 | 11 | ai3 11-12,16 | PX58 | 11 | ai3 3-6,16 |

| BYTE NUMBER 4 / latch pulse ic 19,11 ai3 | | | BYTE NUMBER 3 / latch_pulse ZCLE6_SSB | | |
|---|---|---|---|---|---|
| Potmeter X6 | 4094 IC 20 ai3 | DAC08 | gain ctrl Y6 | 4094 IC 13 ai3 | 4053 IC 14 ai3 |
| Dedication | TX Telephone attenuation ctrl | | Dedication | RX Telephone gain control | |
| serial in from | ai2 4094 IC 8 pin 10 | | serial in from | ai2 4094 IC20 pin 10 | |
| Bit description | 4094 pin nr | DAC08 ic,pin | Bit description | 4094 pin nr | 4053 ic,pin |
| PX61 | pin 4 lsb | ai2 15-18, 9msb | ISY60 | pin 4 lsb | ai3 14,9 lsb |
| PX62 | 5 | ai2 15-18,10 | ISY61 | 5 | ai3 14,11 |
| PX63 | 6 | ai2 15-18,11 | ISY62 | 6 | ai3 14,10 |
| PX64 | 7 | ai2 15-18,12 | ISY63 | 7 | ai3 14,6 |
| PX65 | 14 | ai2 15-18,13 | - | 14 | - |
| PX66 | 13 | ai2 15-18,14 | - | 13 | - |
| PX67 | 12 | ai2 15-18,15 | - | 12 | - |
| PX68 | 11 | ai2 15-18,16 | - | 11 | - |

| BYTE NUMBER 2 / latch pulse ZCLE5_SSB | | | BYTE NUMBER 1 / latch_pulse ZCLE6_SSB | | |
|---|---|---|---|---|---|
| gain ctrl Y5 | 4094 IC 1 ai3 | 4053 IC 2 ai3 | Potmeter Y6 | 4094 IC 21 ai3 | DAC 08 |
| Dedication | Mic operator gain control | | Dedication | RX telephone attenuation ctrl | |
| serial in from | ai2 4094 IC 13 pin 10 | | serial in from | ai3 4094 IC1 pin 10 | |
| Bit description | 4094 pin nr | 4053 ic,pin | Bit description | 4094 pin nr | DAC 08 ic,pin |
| ISY50 | pin 4 lsb | ai3 2,9 lsb | PY61 | pin 4 lsb | ai3 23-24, 9msb |
| ISY51 | 5 | ai3 2,11 | PY62 | 5 | ai3 23-24,10 |
| ISY52 | 6 | ai3 2,10 | PY63 | 6 | ai3 23-24,11 |
| ISY53 | 7 | ai3 2,6 | PY64 | 7 | ai3 23-24,12 |
| - | 14 | - | PY65 | 14 | ai3 23-24,13 |
| - | 13 | - | PY66 | 13 | ai3 23-24,14 |
| - | 12 | - | PY67 | 12 | ai3 23-24,15 |
| - | 11 | - | PY68 | 11 | ai3 23-24,16 |

# 14. SERIAL SHIFT REGISTER CHAIN 2 FOR OUTPUT

| BYTE NUMBER 5 | | | BYTE NUMBER 4 | | |
|---|---|---|---|---|---|
| Hex display | 4094 IC 44 | display LD2 | Hex display | 4094 IC 43 | display LD1 |
| Dedication | : Left hex display | | Dedication | : Right hex display | |
| serial in from | : SERDATO_SSB | | serial in from | : 4094 IC 44 PIN 10 | |
| 3) segment bit | 4094 pin nr | display pin nr | segment bit | 4094 pin nr | display pin nr |
| A1 | pin 4 lsb | 10 | A2 | pin 4 lsb | 10 |
| B1 | 5 | 9 | B2 | 5 | 9 |
| C1 | 6 | 8 | C2 | 6 | 8 |
| D1 | 7 | 5 | D2 | 7 | 5 |
| E1 | 14 | 4 | E2 | 14 | 4 |
| F1 | 13 | 1 | F2 | 13 | 1 |
| G1 | 12 | 2 | G2 | 12 | 2 |
| DP1 | 11 | 7 | DP2 | 11 | 7 |

3) Active Low . Resetting the display segment bit switches the particular segment led on .

| BYTE NUMBER 3 | | | | | |
|---|---|---|---|---|---|
| User outputs | 4094 IC 42 | | | | |
| Dedication | : Opto couplers of user outputs | | | | |
| Serial in from | : 4094 IC 43 PIN 10 | | | | |
| bit description | 4094 pin nr | optocoupler | | | |
| 4) UOB0 | pin 4 lsb | U51.A | | | |
| UOB1 | 5 | U51.B | | | |
| UOB2 | 6 | U51.C | | | |
| UOB3 | 7 | U51.D | | | |
| UOB4 | 14 | U52.A | | | |
| UOB5 | 13 | U52.B | | | |
| UOB6 | 12 | U52.C | | | |
| UOB7 | 11 | U52.D | | | |

4) Resetting the optocoupler bit switches the optocoupler transistor on.

| BYTE NUMBER 2 | | | BYTE NUMBER 1 | | |
|---|---|---|---|---|---|
| Vox threshold | 4094 IC 41 | DAC08 IC 10 | Vox attack | 4094 IC 40 | DAC08 IC 9 |
| Dedication | : Vox threshold ctrl DAC | | Dedication | : Vox spike immunity ctrl DAC | |
| serial in from | : 4094 IC 42 PIN 10 | | serial in from | : 4094 IC 41 PIN 10 | |
| bit description | 4094 pin nr | DAC 08 ic-pin | bit description | 4094 pin nr | DAC 08 ic-pin |
| VXTB0 | pin 4 lsb | 9 msb | VXSIB0 | pin 4 lsb | 9 msb |
| VXTB1 | 5 | 10 | VXSIB1 | 5 | 10 |
| VXTB2 | 6 | 11 | VXSIB2 | 6 | 11 |
| VXTB3 | 7 | 12 | VXSIB3 | 7 | 12 |
| VXTB4 | 14 | 13 | VXSIB4 | 14 | 13 |
| VXTB5 | 13 | 14 | VXSIB5 | 13 | 14 |
| VXTB6 | 12 | 15 | VXSIB6 | 12 | 15 |
| VXTB7 | 11 | 16 | VXSIB7 | 11 | 16 |

# 15. SERIAL SHIFT REGISTER CHAIN 3 FOR INPUT

| BYTE NUMBER 1 | | | BYTE NUMBER 2 | | |
|---|---|---|---|---|---|
| User inputs | 7597 IC 37 | | dipswitch | 7597 IC 34 | |
| Dedication | : Opto couplers of user inputs | | Dedication | : DIPSWITCH | |
| Serial in from | : 7597 IC 34 PIN9 | | serial in from | : 7597 IC 37 PIN9 | |
| bit description | 7597 pin nr | optocoupler | bit description | 7597 pin nr | dispswitch |
| UIB1 | pin 15 lsb | U38 .A | B_0 | pin 15 lsb | DS1 |
| UIB2 | 1 | U38 .B | B_1 | 1 | DS2 |
| UIB3 | 2 | U38 .C | B_2 | 2 | DS3 |
| UIB4 | 3 | U38 .D | B_3 | 3 | DS4 |
| UIB5 | 4 | U39 .A | B_4 | 4 | DS5 |
| UIB6 | 5 | U39 .B | B_5 | 5 | DS6 |
| UIB7 | 6 | U39 .C | B_6 | 6 | DS7 |
| UIB8 | 7 | U39 .D | B_7 | 7 | DS8 |

| BYTE NUMMER 3 | | | | | |
|---|---|---|---|---|---|
| User inputs | 7597 IC 36 | | | | |
| Dedication | : Test inputs | | | : | |
| serial in from | : + 5 Volt | | | : | |
| bit description | 7597 pin nr | Testpin | | | |
| B_0 | pin 15 lsb | ITB2_0 | | | |
| B_1 | 1 | ITB2_1 | | | |
| B_2 | 2 | ITB2_2 | | | |
| B_3 | 3 | ITB2_3 | | | |
| B_4 | 4 | ITB2_4 | | | |
| B_5 | 5 | ITB2_5 | | | |
| B_6 | 6 | ITB2_6 | | | |
| B_7 | 7 | ITB2_7 | | | |